Reference Clock Jitter and Data Jitter

Ransom Stephens, Ph.D.

Abstract:

Reference clock jitter sets the ultimate limit on the bit error ratio of a serial data system. The traditional techniques for quantifying jitter on clock signals don't help system designers estimate the clock's contribution to the total jitter defined at a bit error ratio. New techniques are being introduced to model how transmitters and receivers use reference clocks so that the system RJ and DJ attributable to the reference clock can be measured and maximums specified. This installment of Jitter 360 shows how reference clock jitter affects data jitter at each point in the system and describes techniques for its analysis.

We've seen that the different types of jitter are predominantly generated in specific components of the network. For example, Data Dependent Jitter (DDJ) is generated in the transmission path; Periodic Jitter (PJ) is caused by electromagnetic interference of one sort or another; and Random Jitter (RJ) is caused by "the combination of a huge number of sources, each of very small magnitude" (lifted from Part 3 of this series, *All About the Acronyms*). Most of those very small RJ sources originate in the oscillator that drives the reference clock of the transmitter.

As data rates get higher, jitter budgets get tighter, and we can no longer afford to lump jitter caused by the reference clock under "transmitter jitter." As rates surpass 2 Gb/s more and more standards bodies are providing explicit specifications for reference clock jitter and the new specifications are not easily related to the numbers recorded on most data sheets.

Figure 1 is a block diagram of a serial-data system. The *four* primary components are the transmitter, transmission path, receiver, and reference clock. The role of the reference clock is to define the timing of logic transitions at the transmitter and to provide a reference for setting the time-delay of the sampling point at the receiver. There are two types of clock systems. In embedded clock systems the only clock information available to the receiver is embedded in the data; in this case the dashed line in Figure 1 is not connected. In distributed clock systems, the dashed line in Figure 1 connects the reference clock to the receiver.

In this edition of Jitter 360, we'll see how RJ is generated in oscillators, how reference clock jitter propagates onto data jitter, and we'll have a look at how reference clocks can be evaluated in the emerging high rate serial-data standards.

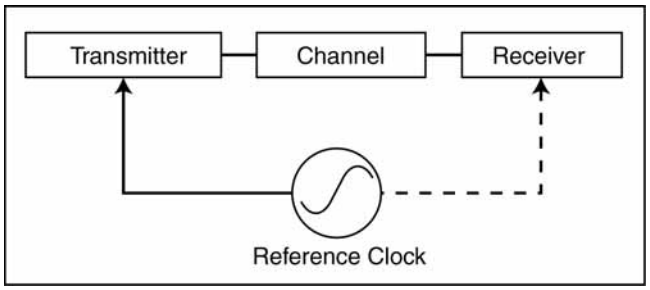

Figure 1: Serial-data straw diagram emphasizing the role of the reference clock.

Oscillators

The oscillator, whether based on an inexpensive LC circuit or a crystal, provides the periodic structure on which a digital system is based. The parameters used to describe oscillators are easily defined by using the example of an LRC circuit shown, Figure 2.

Resonant frequency: $\omega_R = \sqrt{\frac{1}{LC} - \left(R/2L\right)^2} \approx \frac{1}{\sqrt{LC}}$

Damping factor: $\zeta = R/2L$

Bandwidth: $\Delta f = \frac{\zeta}{\pi} = \frac{R}{2\pi L}$

Quality: $Q = \frac{f_R}{\Delta f} = \frac{1}{R}\sqrt{\frac{L}{C}}$

Figure 2: A simple oscillator and typical parameters.

The highest quality oscillators are based on crystals. Crystal oscillators, Figure 3, are composed of media, like quartz, which have easily excited piezoelectric properties. Stable oscillations are generated through a simple sequence based on the fact that any excitation will have its greatest response at the crystal's resonant frequency. First, random noise is applied to the crystal. The response is amplified and a feedback loop generates subsequent crystal response that builds at the resonant frequency. The output

amplitude quickly stabilizes by virtue of either its own self-limiting nonlinearities or a reduction in amplifier gain. Figure 4 shows the spectrum of the settling behavior of an oscillator; notice the excitation of harmonic spurs.

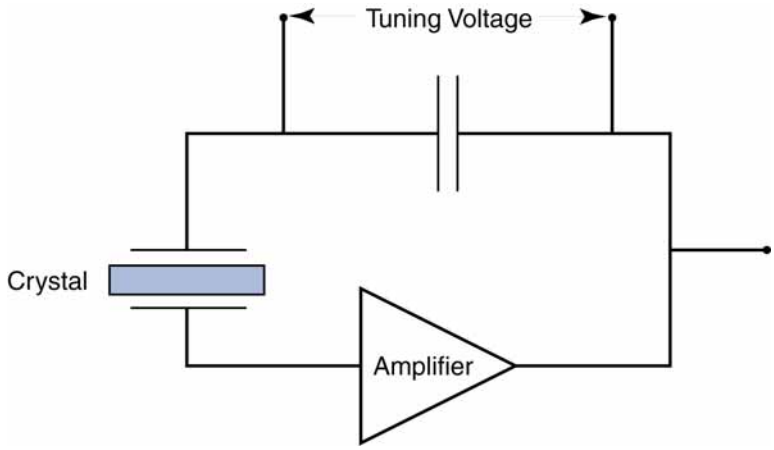

Figure 3: Crystal oscillator [circuit diagram]

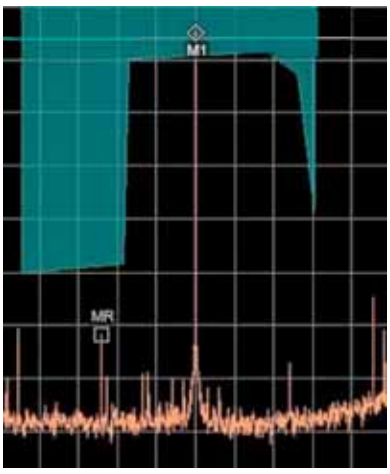

Figure 4: Spectrum of an oscillator as it settles.

The crystal's resonant frequency is determined primarily by its geometry – size, shape and density – which varies slightly with temperature, pressure, humidity, and applied voltage. Figure 5a shows an ideal oscillator spectrum and Figure 5b a spectrum including white noise. The nonzero width of the resonance is the dominant source of near-carrier noise. Tens of kHz above resonance, crystal vibrations can cause spurs at integer multiples of the difference between the vibration and carrier frequencies resulting in both periodic noise and jitter, Figure 5c. Far from the carrier the dominant noise effects are caused by

inadequacies in the oscillator feedback loop such as impedance mismatches and power-supply feed-through that sits atop the white noise background.

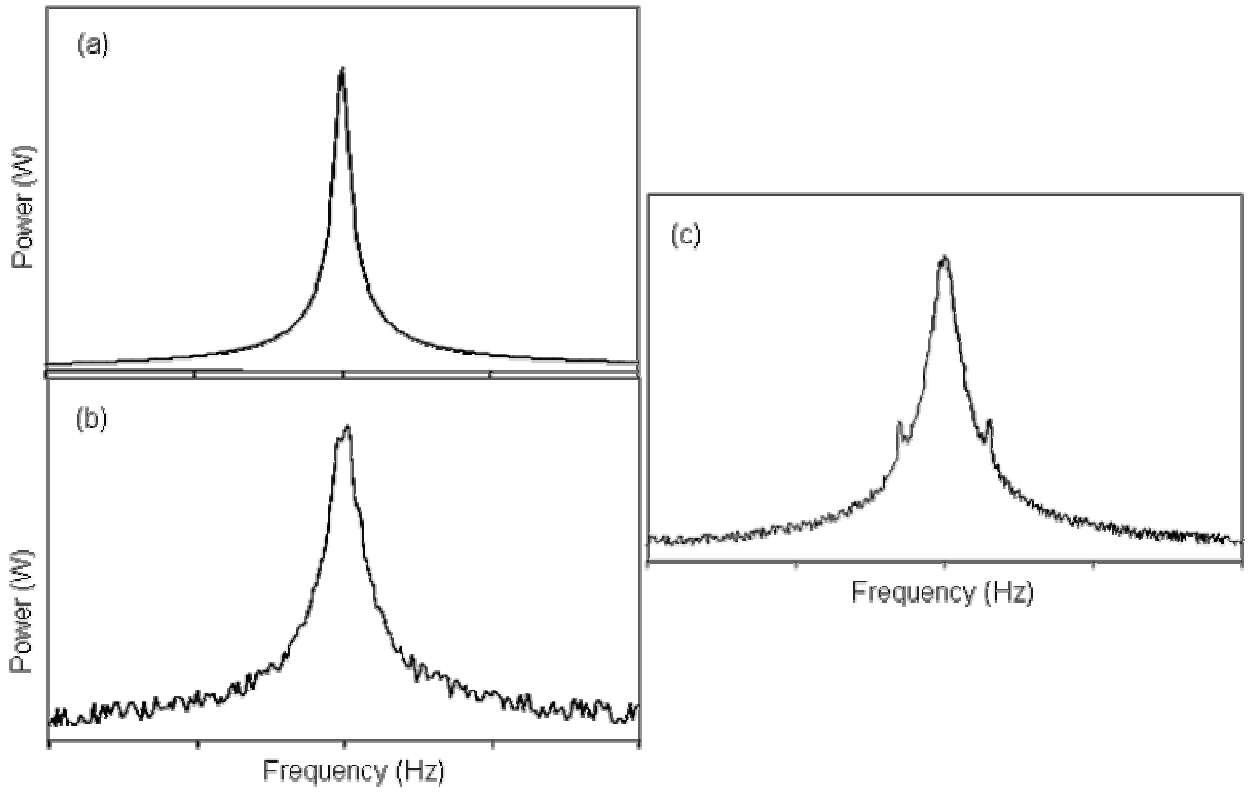

Figure 5: Oscillator or clock signal in the frequency domain, (a) an ideal Lorentzian resonance, (b) with white noise, (c) with spurs from crystal vibrations.

An ideal oscillator signal is a sinusoid with unvarying amplitude, A, and frequency, f:

$$\psi(t) = A \sin(2\pi ft)$$

a real oscillator has both amplitude noise, $\delta A(t)$ and phase noise, $\varphi(t)$

$$\psi(t) = (A + \delta A(t)) \sin(2\pi ft + \varphi(t)).$$

Random jitter from the oscillator is ultimately caused by a combination of phase noise and amplitude noise. Up to a factor of 2π, the phase noise, $\varphi(t)$ is precisely timing noise, the horizontal fluctuation of the signal. Amplitude noise, $\delta A(t)$, is the vertical fluctuation of the signal. Recall from Part 4: *Jitter Analysis in*

Systems With Crosstalk, that amplitude noise, $\delta A(t)$, introduces jitter as well as voltage noise as a consequence of the signal's nonzero rise/fall times.

The phase noise component of RJ originates in the continuum background of the frequency spectrum (a result exploited by the best jitter analysis algorithms which equate the rms jitter-frequency noise with the width of the RJ distribution, σ).

Of the different types of jitter, RJ is the most intractable from the design standpoint. Still, RJ can be reduced by understanding its primary sources. Excessively broad resonance structures can be caused by vibration, mechanical shock, or temperature variations which result in small random variations in the resonant frequency.

The Lorentzian shape of the resonance curve is caused by "flicker" – a process that appears in phenomena ranging from the behavior of stock prices to the behavior of stars – is related to the way that oscillations propagate through different regions of the crystal.

If the shape of the peak is asymmetric, flat-topped, or otherwise non-Lorentzian, then something fundamental is probably wrong with the crystal itself.

Noisy electronics in the oscillator circuit, usually from the amplifier, can cause the resonant curve to widen at its base.

White noise is a flat continuous background that is caused primarily by thermal noise in resistors, inductors, diodes and so forth.

Unfortunately, RJ cannot be eliminated by use of a limiting amplifier. Nor can RJ that is close to the carrier be reduced by filtering. Conversely, jitter that is far from the carrier, primarily caused by white noise, can be filtered.

At the Transmitter

To define the timing of logic transitions, the transmitter requires a data-rate clock signal. To convert the reference clock to a data-rate clock, transmitters typically use frequency multiplying Phase Locked Loops (PLLs). The important thing to remember is that frequency multiplication amplifies the phase noise by the *square* of the multiplication factor. That is, the phase noise increases by 20 dB for every 10 dB of multiplication.

The 20 dB increase in phase noise for each 10 dB of multiplication is the primary reason that high data rate standards address the jitter caused by reference clocks independent of other sources. There are two options: use higher quality oscillators or be very careful in how reference clocks are specified.

The frequency multiplying PLL, Figure 6a, introduces additional RJ, primarily from its Voltage Controlled Oscillator (VCO). Nonlinearities in the PLL are a principle cause of Duty Cycle Distortion (DCD).

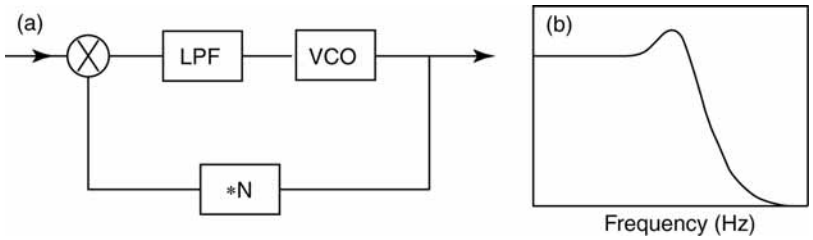

Figure 6: PLL Multipler (a) block diagram, (b) frequency response.

On the other hand, the PLL also acts as a filter. Figure 6b shows a typical PLL frequency response, just as in Part 5, *Clock Recovery in Serial-Data Systems*, the question begs: What part of the jitter frequency spectrum contributes to the bit error ratio? Remember, the only reason we care about jitter is that it causes errors.

At the Receiver

The reference clock plays different roles at the receiver. All imperfections on the reference clock that make it past the filtering effect of the transmitter PLL-multiplier are on the data recovered at the receiver.

As discussed at length in Part 5, *Clock Recovery in Serial-Data Systems*, the data-rate clock is recovered at the receiver either with or without the assistance of a distributed reference clock. The primary issue, from the BER standpoint, is whether or not the jitter on the recovered clock tracks the jitter on the data. Just as the bandwidth of the receiver's clock recovery circuit determines the frequencies of jitter that are tracked, the bandwidth of the transmitter's PLL-multiplier determines the reference clock jitter that makes it through to the data. The ideal situation is to have a narrow bandwidth multiplier at the transmitter and a wide bandwidth clock recovery at the receiver. This way, little jitter makes it from the clock to the data and the jitter that does make it is also on the recovered clock so that the sampling point jitters in phase with the data.

There is an added complication when the reference clock is distributed to the receiver. For example, in the Phase Interpolator (PI) based clock recovery circuit, Figure 7, there is another PLL multiplier. The frequency response of the receiver's multiplier is likely to have a different frequency response than the one at the transmitter. Mismatched multipliers have the potential to introduce small amounts of jitter to the recovered clock that are not on the data.

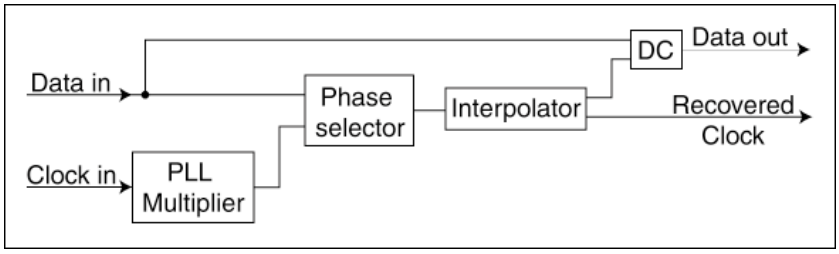

Figure 7: Phase interpolator based receiver.

Analyzing Clock Jitter

It is difficult to translate the quantities that traditionally appear on clock data sheets – peak-to-peak phase jitter, period jitter, and cycle-to-cycle jitter – to the only relevant question: What impact does the clock have on the system Bit Error Ratio?

The most useful traditional clock evaluation is the phase noise spectrum. If the bandwidth of the transmitter clock multiplier and the bandwidth of the receiver clock recovery circuit are both known, then at least we can determine whether the bulk of the phase noise can affect the BER. This is the purpose of phase noise mask tests.

The increased use of RJ and DJ to estimate TJ(BER) encourage clock vendors to quote RJ and DJ under the extreme transmitter bandwidths of both the transmitter-multiplier and receiver clock-recovery specified for different technologies. This way, as shown in Part 1, *The Meaning of Total Jitter*, the system TJ(BER) budget can be estimated for different transmitter/channel/receiver/reference clock combinations.

Real time oscilloscopes and spectrum analyzers can be used to assemble data from a clock signal to evaluate the relevant RJ and DJ by applying the transfer functions of the worst-case transmitter-multiplier/receiver-clock-recovery combinations described by the standard.

The trace of a real time oscilloscope is used to determine a data set of the timing of logic transitions, $\{t_n\}$. Numerical techniques from Digital Signal Processing (DSP) are then applied to the data to simulate the

transmitter-multiplier and receiver clock-recovery responses. Similarly, the frequency spectrum from a real time spectrum analyzer can be processed by applying the same techniques in the frequency domain. In either case, the usual jitter analysis techniques can then be applied to the simulation to determine the effective worst-case RJ and DJ that the clock may contribute to a system. With the RJ and DJ in hand, the dual-Dirac model (see Part 2, *What the Dual-Dirac Model is and What it is Not*) can be used to estimate the reference clock contribution to the overall system BER,

$$TJ(BER) = 2Q_{BER} \times RJ + DJ.$$

Conclusion

Reference clock jitter plays such a key role in the ultimate BER of serial-data systems that the worst case RJ/DJ for each application should be reported on clock data sheets. This would allow design engineers to assemble systems with predictable TJ(BER).

The reference clock itself is a primary source of RJ. The shape of the oscillator resonance and the phase noise spectrum can be used for diagnostics that can reduce RJ. The reference clock can also contribute PJ and DCD.

The transmitter usually multiplies a low rate reference clock up to the data rate. The PLL multiplier includes a VCO that contributes additional jitter and the multiplication process itself amplifies the jitter by the square of the multiplication factor.

The combination of a narrow bandwidth multiplier at the transmitter and wide bandwidth clock recovery at the receiver produces a system with the lowest BER.

Reference clocks can be evaluated using DSP techniques on data provided by real-time oscilloscopes or spectrum analyzers to simulate the effect of different transmitter PLL-multiplier/receiver-clock-recovery schemes resulting in RJ and DJ estimates that can be used to estimate the overall system TJ(BER).